Fig. 1
PRIOR ART

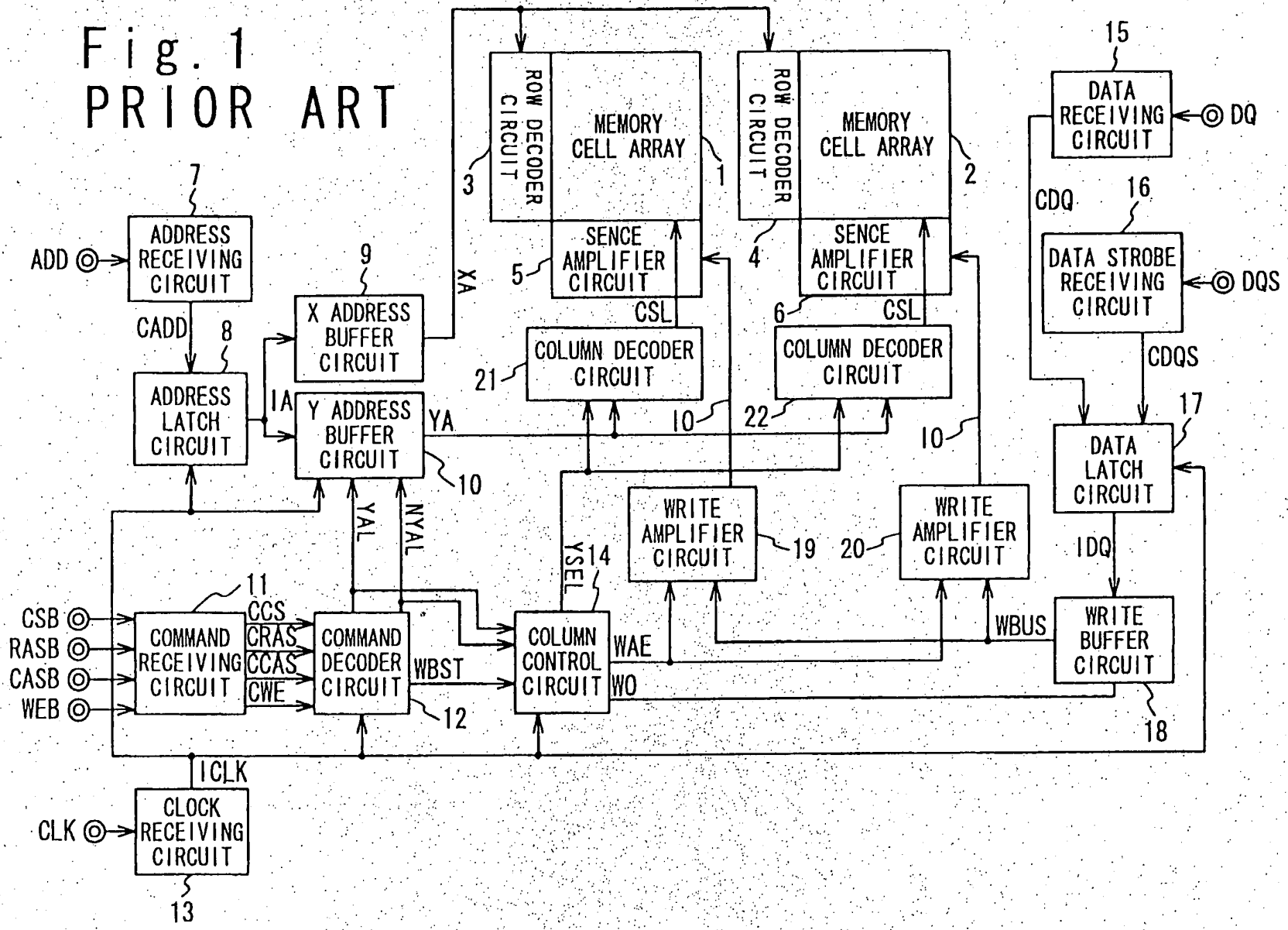


Fig. 2 PRIOR ART

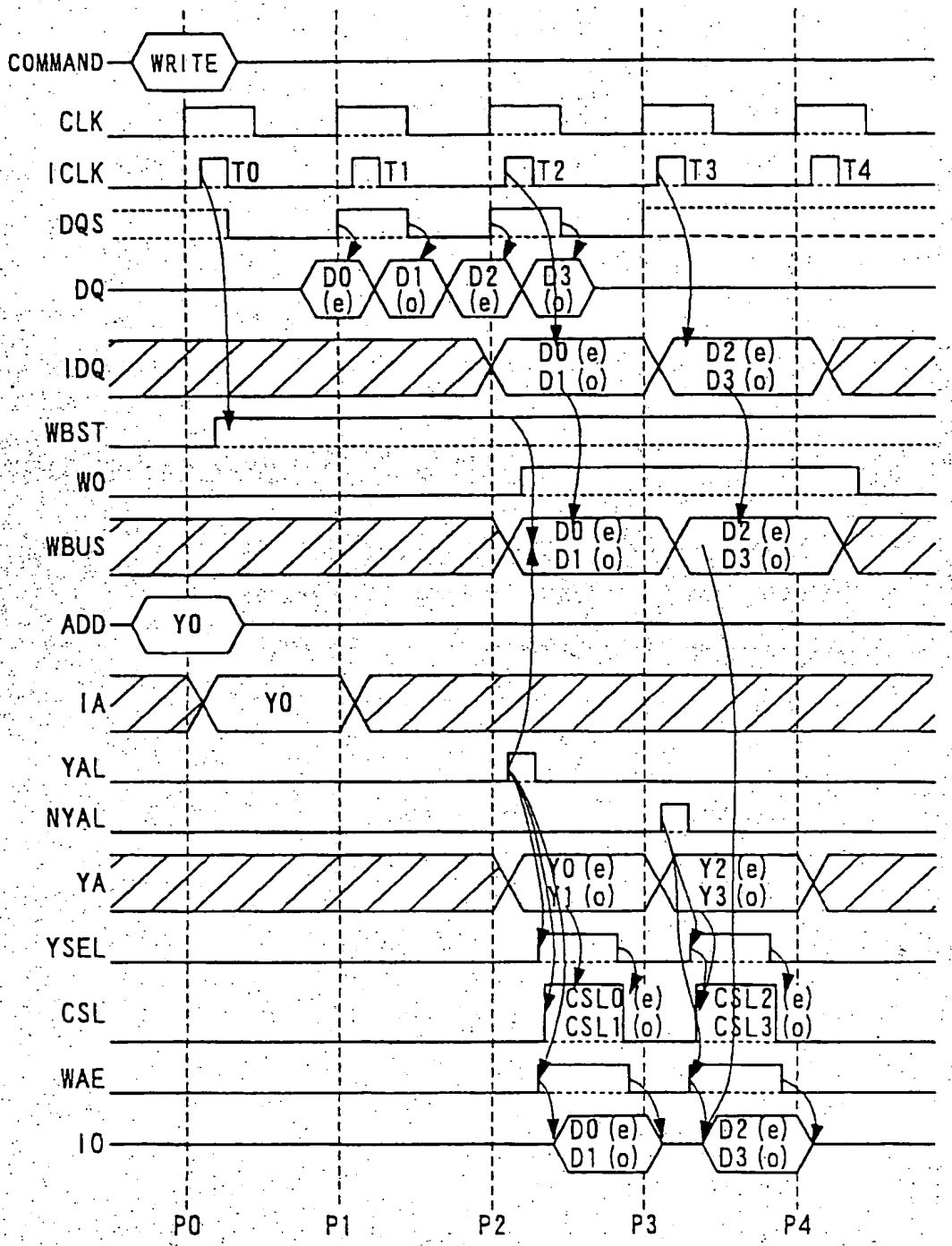


Fig. 3 PRIOR ART

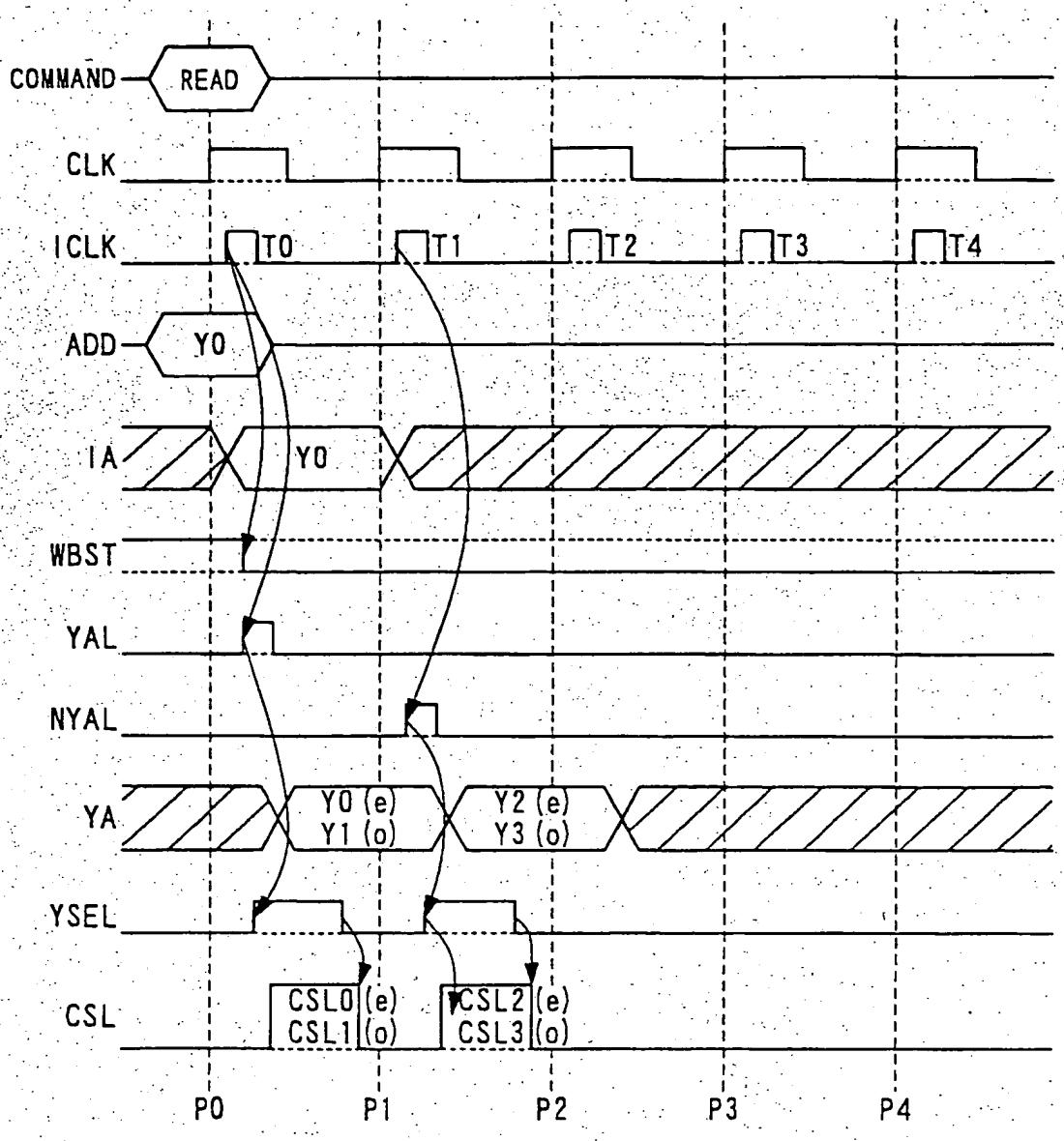


Fig. 4
PRIOR ART

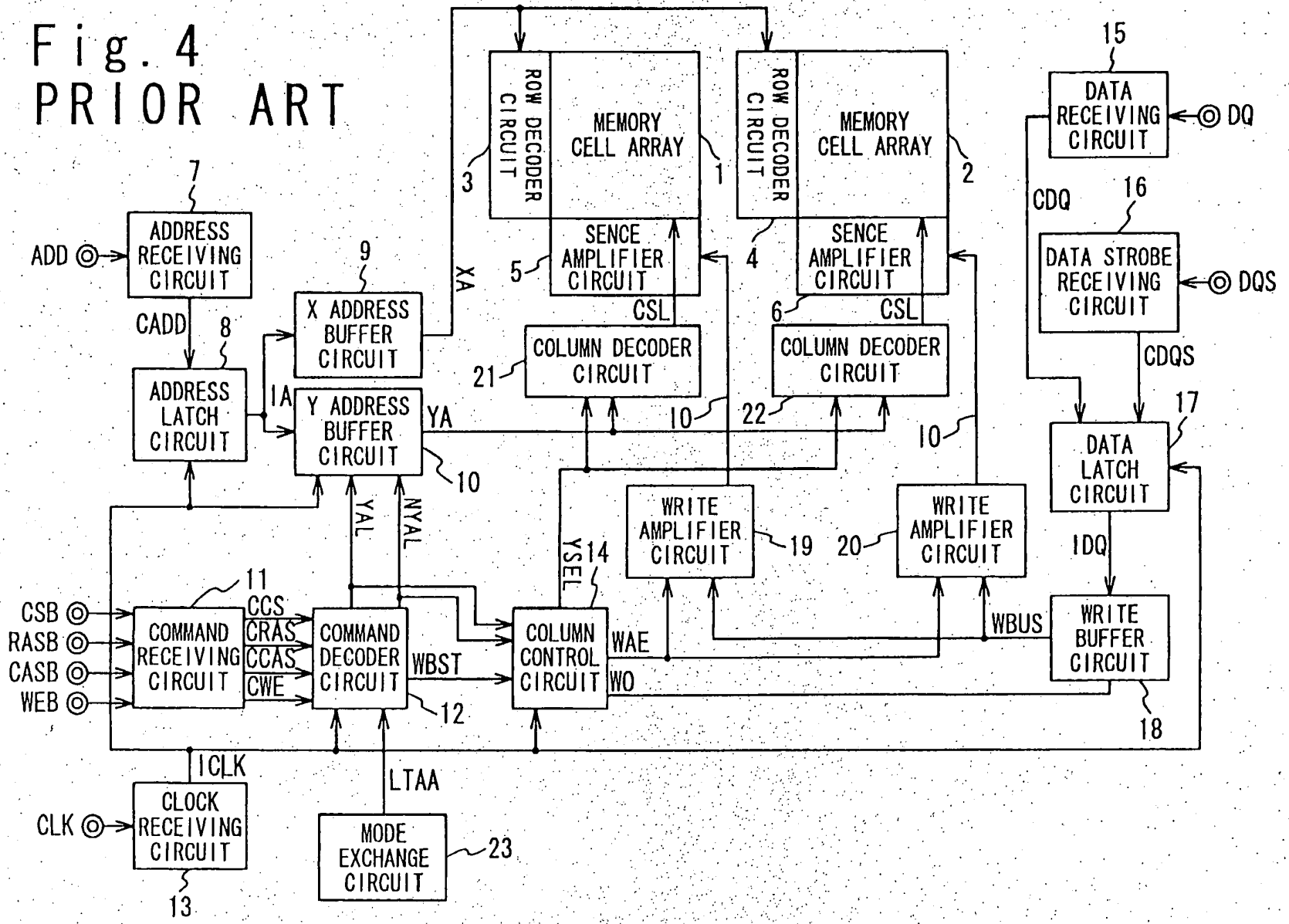


Fig. 5 PRIOR ART

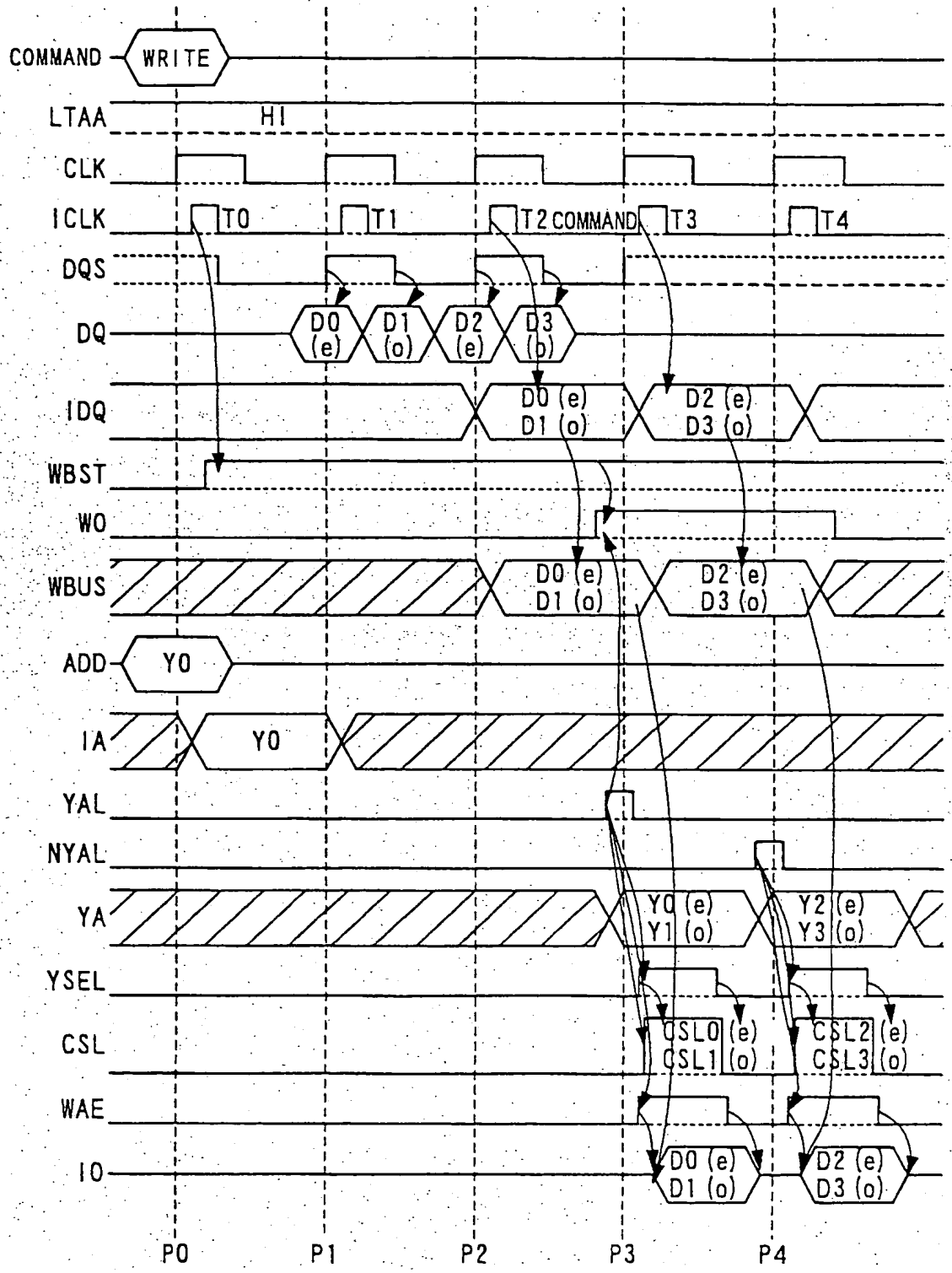


Fig. 6 PRIOR ART

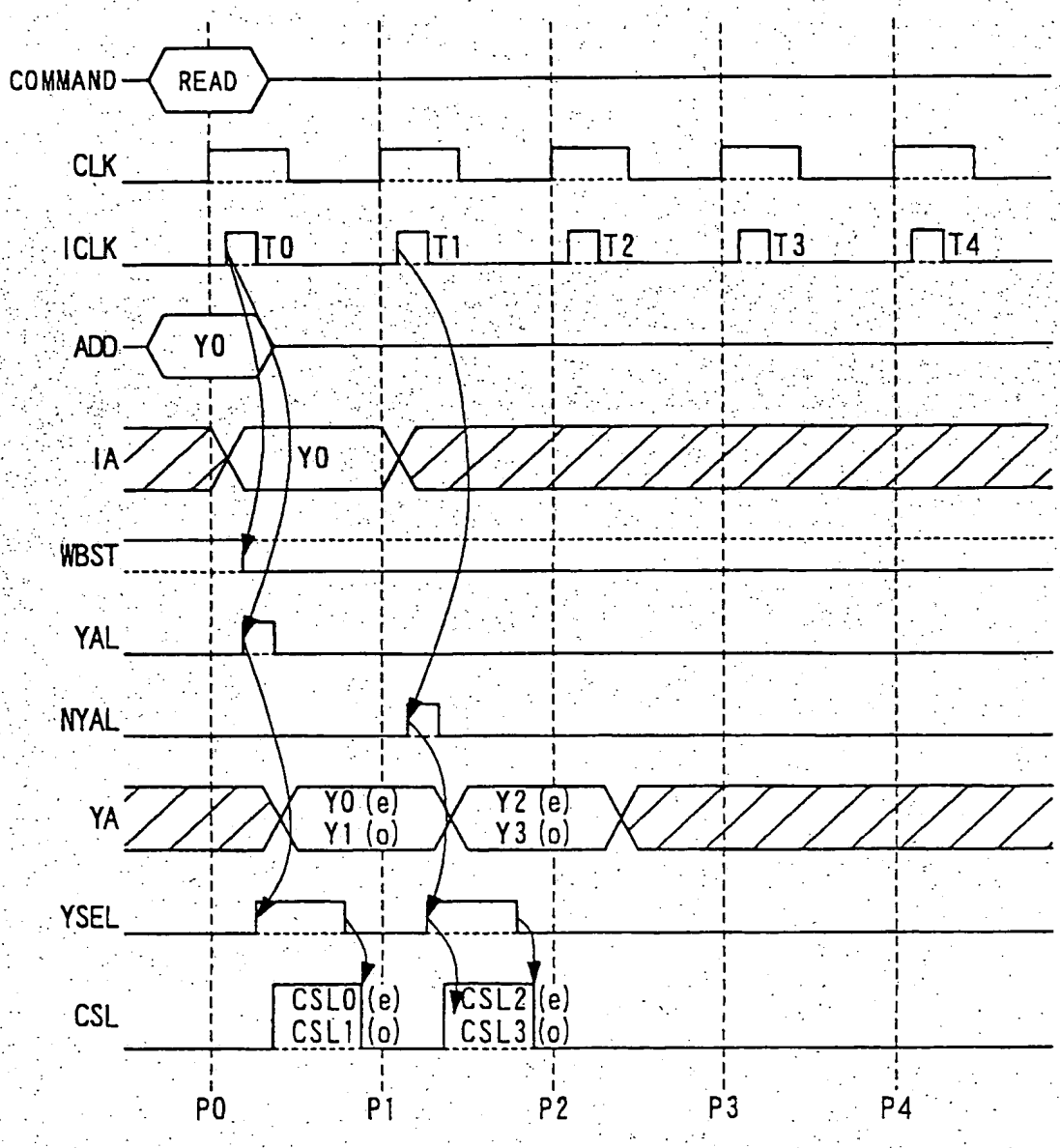


Fig. 10

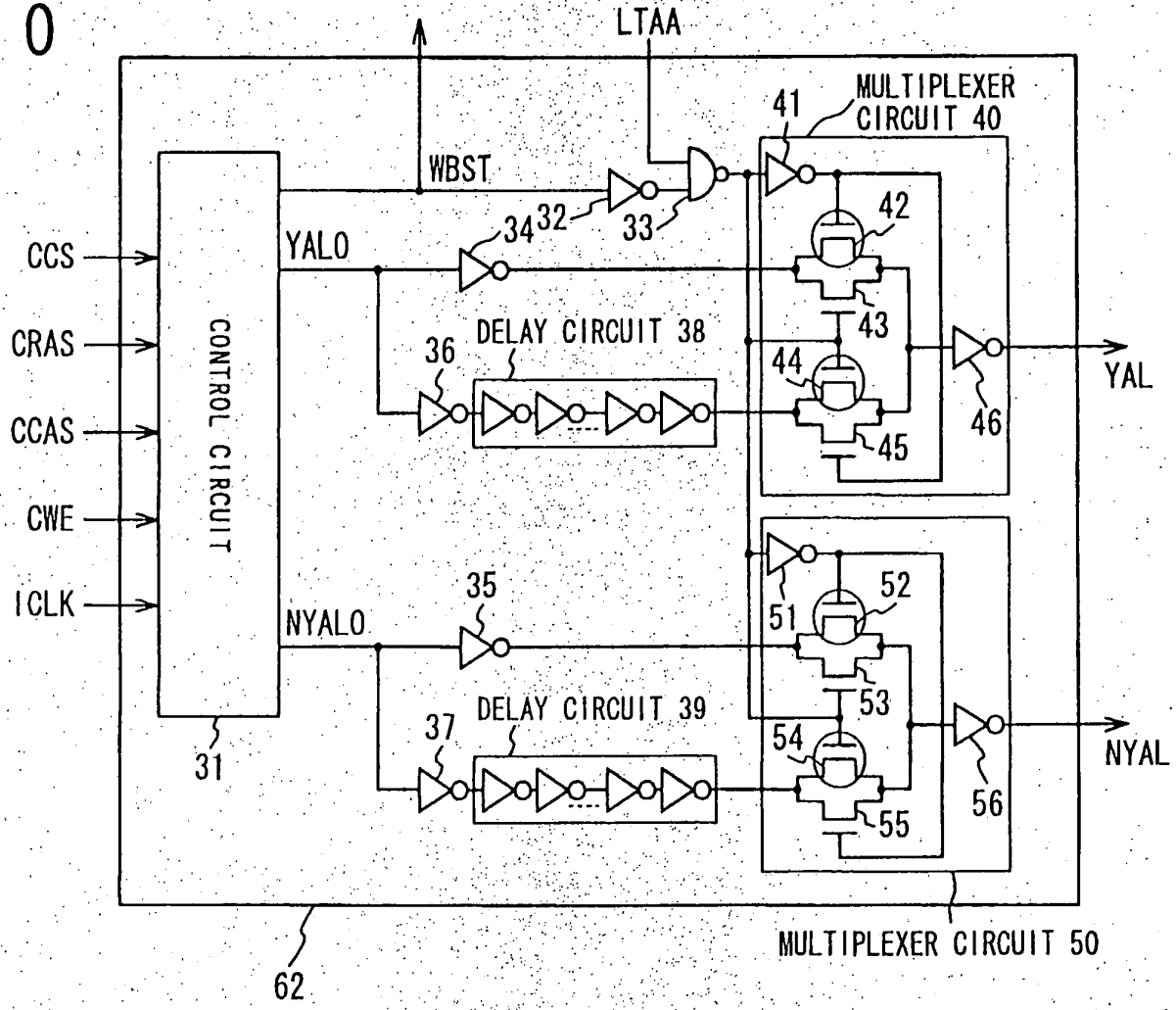

LTAA
MULTIPLEXER CIRCUIT 40
41
WBST
42
34
32
33
CCS
YALO
43
CRAS
DELAY CIRCUIT 38
36
44
YAL
CCAS
46
45
CWE
CONTROL CIRCUIT
ICLK
35
52
51
NYALO
53
DELAY CIRCUIT 39
37
54
NYAL
56
55
31
MULTIPLEXER CIRCUIT 50
62

Fig. 9

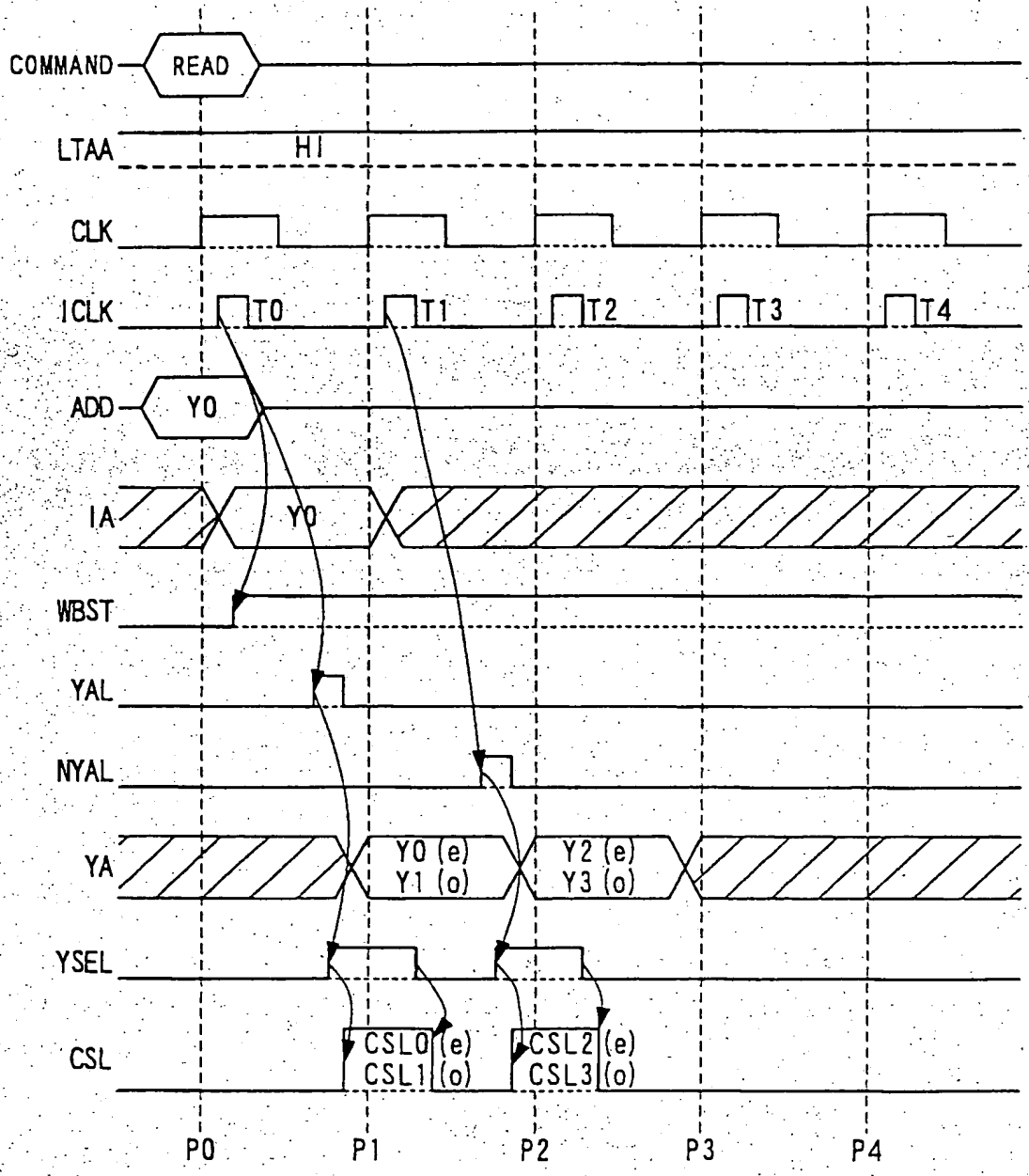

COMMAND
READ
LTAA
HI
CLK
ICLK
T0
T1
T2
T3
T4
ADD
Y0
IA
Y0
WBST
YAL
NYAL
YA
Y0 (e)
Y1 (o)
Y2 (e)
Y3 (o)
YSEL
CSL
CSL0 (e)
CSL1 (o)
CSL2 (e)
CSL3 (o)
P0
P1
P2
P3
P4

Fig. 8

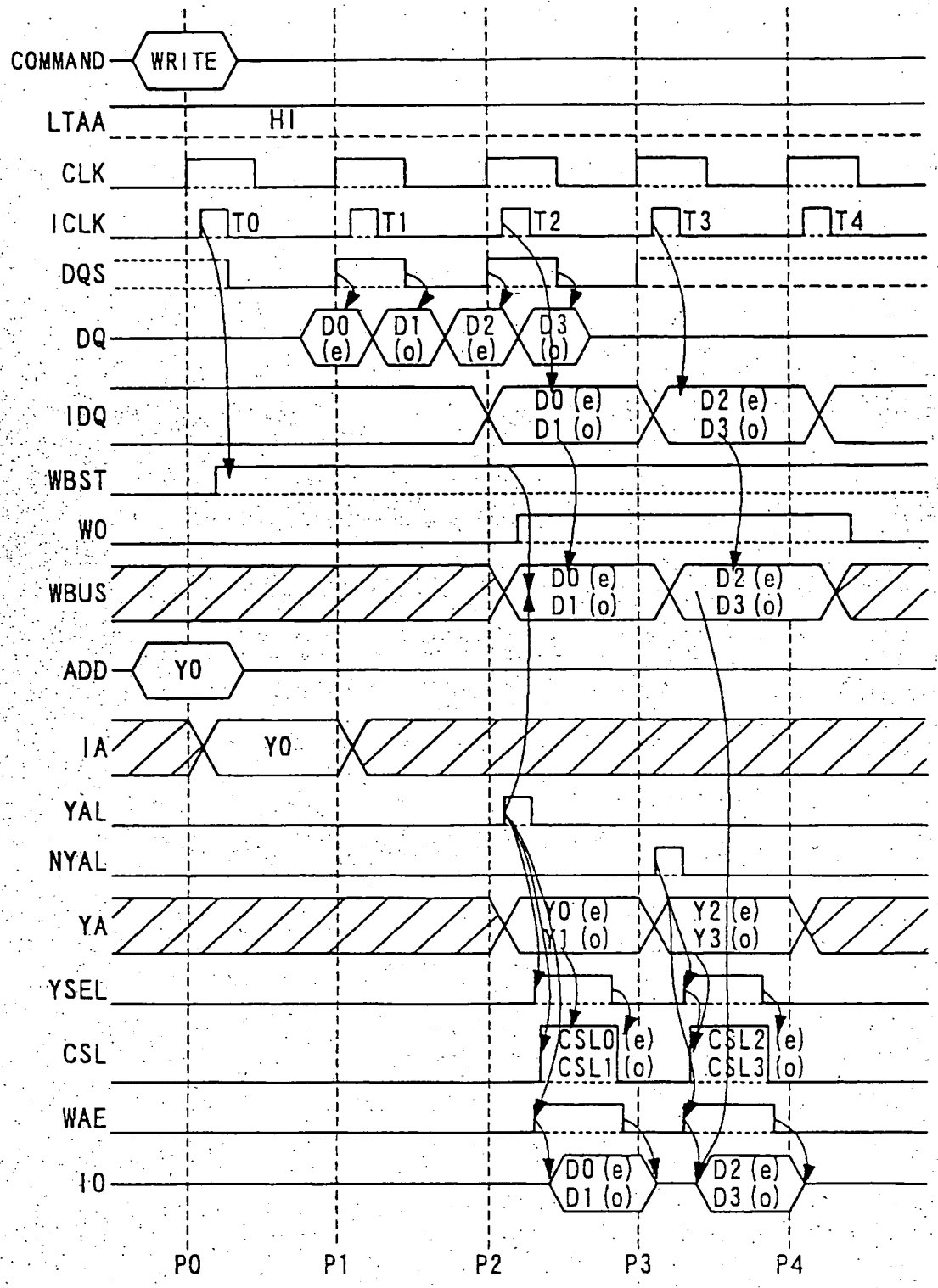
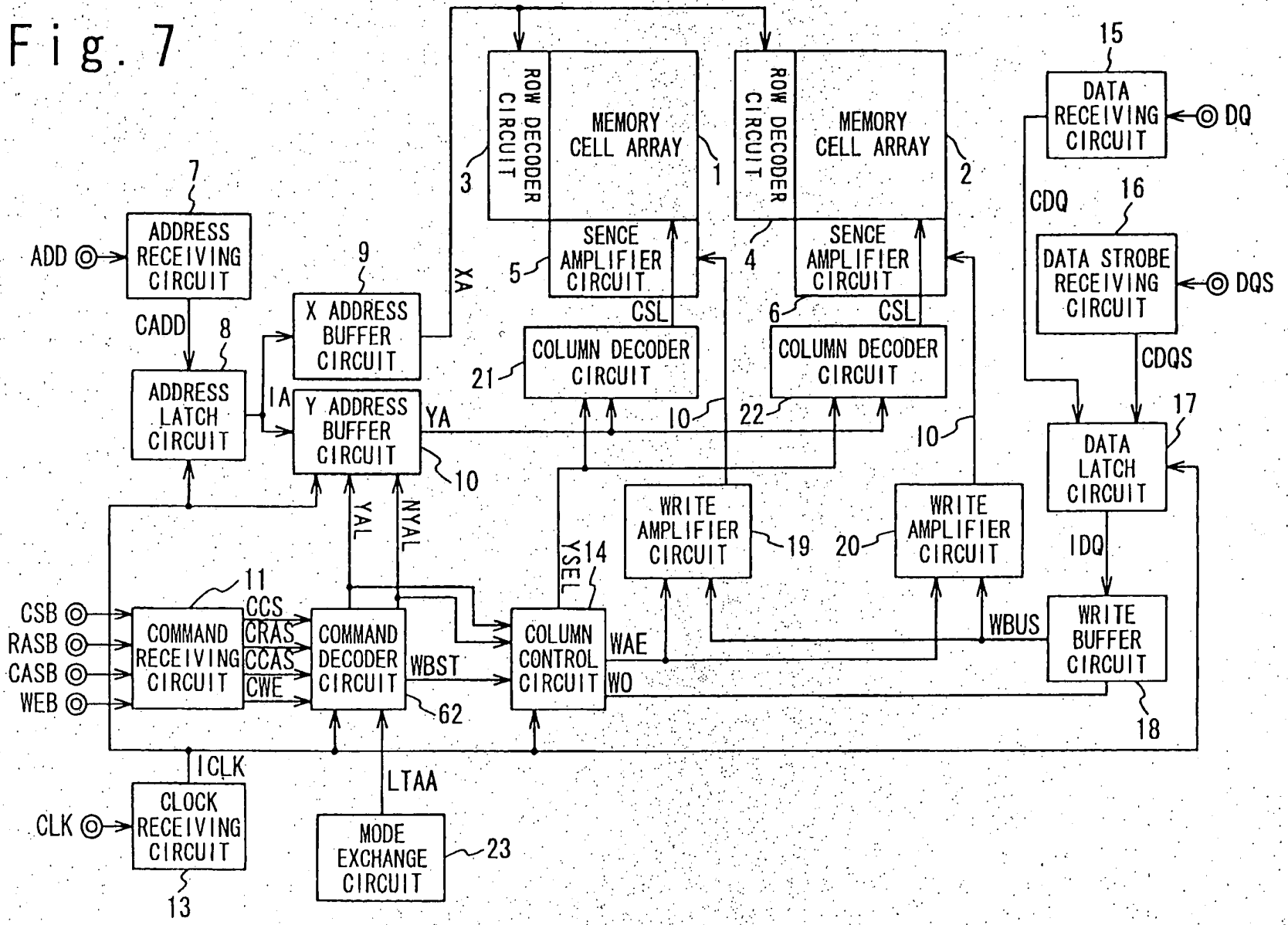

COMMAND
WRITE
LTAA
HI
CLK
ICLK
T0
T1
T2
T3
T4
DQS
DQ
D0 (e)
D1 (o)
D2 (e)
D3 (o)
IDQ
D0 (e)
D1 (o)
D2 (e)
D3 (o)
WBST
WO
WBUS
D0 (e)
D1 (o)
D2 (e)
D3 (o)
ADD
Y0
IA
Y0
YAL
NYAL
YA
Y0 (e)
Y1 (o)
Y2 (e)
Y3 (o)
YSEL
CSL
CSL0 (e)
CSL1 (o)
CSL2 (e)
CSL3 (o)
WAE
IO
D0 (e)
D1 (o)
D2 (e)
D3 (o)
P0
P1
P2
P3
P4

Fig. 7


ROW DECODER CIRCUIT
MEMORY CELL ARRAY
3
1
2
SENCE AMPLIFIER CIRCUIT
5
4
6
CSL
COLUMN DECODER CIRCUIT
21
10
22
15
DATA RECEIVING CIRCUIT
DQ
CDQ
16
DATA STROBE RECEIVING CIRCUIT
DQS
CDQS
17
DATA LATCH CIRCUIT
IDQ
WRITE BUFFER CIRCUIT
18
WBUS
WRITE AMPLIFIER CIRCUIT
19
20
WAE
WO
COLUMN CONTROL CIRCUIT
14
YSEL
7
ADDRESS RECEIVING CIRCUIT
ADD
CADD
8
ADDRESS LATCH CIRCUIT
IA
9
X ADDRESS BUFFER CIRCUIT
XA
Y ADDRESS BUFFER CIRCUIT
YA
YAL
NYAL
11
CSB
RASB
CASB
WEB
COMMAND RECEIVING CIRCUIT
CCS
CRAS
CCAS
CWE
COMMAND DECODER CIRCUIT
WBST
62
ICLK
CLOCK RECEIVING CIRCUIT
CLK
13
LTAA
MODE EXCHANGE CIRCUIT
23